UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,903,361 B2
APPLICATION NO. : 10/663741
DATED : June 7, 2005
INVENTOR(S) : Terry L. Gilton

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Replace Title Page with attached title page.

Drawings

In the Drawings, substitute the attached set of drawings for those that are in the patent.

Title Page #56

In the U.S. Patent Documents portion of the References Cited section, the following is corrected:

Page 2 Col. 2

"2002/0000668 A1 1/2002 Kozicki et al." should read

--2002/0000666 A1 1/2002 Kozicki et al.--

Title Page in the Other Publications portion of the References Cited section, the following errors are corrected:

Page 1 Col. 2

"Yoji Kawamoto et al., "Ionic Conduction in As_2S_3-Ag_2S, GeS_2-GeS_2-GeS-AG_2S and P_2S_g-Ag_2S Glasses," Journal of Non-Crystalline Solids 20 (1976) 393-404."

Should read

--Yoji Kawamoto et al. "Ionic Conduction in As_2S_3-Ag_2S, GeS_2-GeS_2-GeS-Ag_2S and P_2S_6-Ag_2S Glasses," Journal of Non-Crystalline Solids 20 (1976) 393-404.--;

"El Bouchairi, B.; Bernede, J.C.; Burgaud, P., Propeties of $Ag_{2-x}Se_{1+x/n}$-Si diodes, Thin Solid Films 110 (1983) 107-113."

Should read

Page 4 Col. 2 line 8

--El Bouchairi, B.; Bernede, J.C.; Burgaud, P., Properties of $Ag_{2-x}Se_{1+x/n}$-Si diodes, Thin Solid Films 110 (1983) 107-113.--;

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"Hajto, J.; McAuley, B.; Snell, A.J.; Owen, A.E., Theory of room temperature quantized resistance effects in metal-a-Si:H-metal thin film structuress, J. Non-Cryst. Solids 198-200 (1996) 825-828."

Should read

Page 5 Col. 1 line 34

--Hajto, J.; McAuley, B.; Snell, A.J.; Owen, A.E., Theory of room temperature quantized resistance effects in metal-a-Si:H-metal thin film structures, J. Non-Cryst. Solids 198-200 (1996) 825-828.--;

"Kotkata, M.F.; Afif, M.A.; Labib, H.H.; Hegab, N.A.;Abdel-Aziz, M.M., Memory switching in amorphous GeSeTI chalcogenide semiconductor films, Thin Solid Films 240 (1994) 143-146."

Should read

Page 6 Col. 1 line 1

--Kotkata, M.F.; Afifi , M.A.; Labib, H.H.; Hegab, N.A.;Abdel-Aziz, M.M., Memory switching in amorphous GeSeTI chalcogenide semiconductor films, Thin Solid Films 240 (1994) 143-146.--; and

"McHardy, et al., The dissolution of metals in amorphous chalcogenides and the effect o electrons and ultraviolet radiation, 20 J. Phys. C.: Solid State Phys. pp. 4055-4075 (1987)f."

Should read

Page 6, Col. 1 line 46

--McHardy, et al., The dissolution of metals in amorphous chalcogenides and the effect of electrons and ultraviolet radiation, 20 J. Phys. C.: Solid State Phys. pp. 4055-4075 (1987).--.

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INVENTOR(S) : Terry L. Gilton

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

"Mitokova, M.; Wang, Y.; Boolchand, P., Dual chemical role of Ag as an additive in chalcogenide glasses, Phys. Rev. Lett. 83 (1999) 3848-3851."

Should read

Page 6 Col. 1 line 58

--Mitkova, M.; Wang, Y.; Boolchand, P., Dual chemical role of Ag as an additive in chalcogenide glasses, Phys. Rev. Lett. 83 (1999) 3848-3851.--.

In the Specification, the following errors are corrected:

Column 5:

Line 48, "deposition an" should read --deposition of an--; and

Line 61, "increase" should read --increases--.

Column 6:

Line 4, "increase" should read --increases--; and

Line 5, "decrease" should read --decreases--.

Column 7:

Line 47, "include" should read --includes--.

Column 8:

Line 4, "an local" should read --a local--;

Line 8, "an universal" should read --a universal--;

Line 9, "via to the" should read --via the--; and

Line 12, "to one additional" should read --to additional--.

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INVENTOR(S) : Terry L. Gilton

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims, the following errors are corrected:

Column 8:

Claim 3, line 54, "chacogenide" should read --chalcogenide--;

Claim 4, line 56, "chacogenide" should read --chalcogenide--;

Claim 7, line 61, "chacogenide" should read --chalcogenide--;

Claim 8, line 63, "chacogenide" should read --chalcogenide--; and

Claim 9, line 67, "tantalium" should read --tantalum--.

Column 9:

Claim 10, line 9, "conducive" should read --conductive--;

Claim 12, line 20, "chacogenide" should read --chalcogenide--;

Claim 13, line 22, "chacogenide" should read --chalcogenide--;

Claim 16, line 27, "chacogenide" should read --chalcogenide--;

Claim 17, line 29, "chacogenide" should read --chalcogenide--;

Claim 18, line 34, "tantalium" should read --tantalum--;

Claim 21, line 53, "chacogenide" should read --chalcogenide--; and

Claim 22, line 55, "chacogenide" should read --chalcogenide--.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10:

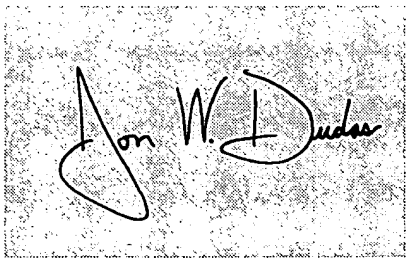
Claim 25, line 2, "chacogenide" should read --chalcogenide--;

Claim 26, line 4, "chacogenide" should read --chalcogenide--; and

Claim 27, line 8, "tantalium" should read --tantalum--.

Signed and Sealed this

Twentieth Day of February, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Gilton

(10) **Patent No.: US 6,903,361 B2**
(45) **Date of Patent: Jun. 7, 2005**

(54) **NON-VOLATILE MEMORY STRUCTURE**

(75) Inventor: **Terry L. Gilton, Boise, ID (US)**

(73) Assignee: **Micron Technology, Inc., Boise, ID (US)**

(*) Notice: **Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.**

(21) Appl. No.: **10/663,741**

(22) Filed: **Sep. 17, 2003**

(65) **Prior Publication Data**

US 2005/0056910 A1 Mar. 17, 2005

(51) **Int. Cl.**[7] **H01L 47/00**
(52) **U.S. Cl.** **257/2**
(58) **Field of Search** 257/2–4, 314–324; 438/257–265

(56) **References Cited**

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(Continued)

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WO	WO 00/48195	8/2000
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OTHER PUBLICATIONS

Yoji Kawamoto et al., "Ionic Conduction in As_2S_3–Ag_2S, GeS_2–GeS_2–GeS–AG_2S and P_2S_5–Ag_2S Glasses," Journal of Non–Crystalline Solids 20 (1976) 393–404.

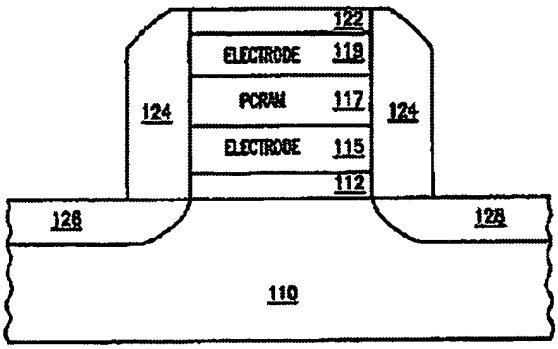
(Continued)

Primary Examiner—Cuong Nguyen
(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky LLP

(57) **ABSTRACT**

A non-volatile memory cell utilizes a programmable conductor random access memory (PCRAM) structure instead of a polysilicon layer for a floating gate. Instead of storing or removing electrons from a floating gate, the programmable conductor is switched between its low and high resistive states to operate the flash memory cell. The resulting cell can be erased faster and has better endurance than a conventional flash memory cell.

30 Claims, 9 Drawing Sheets



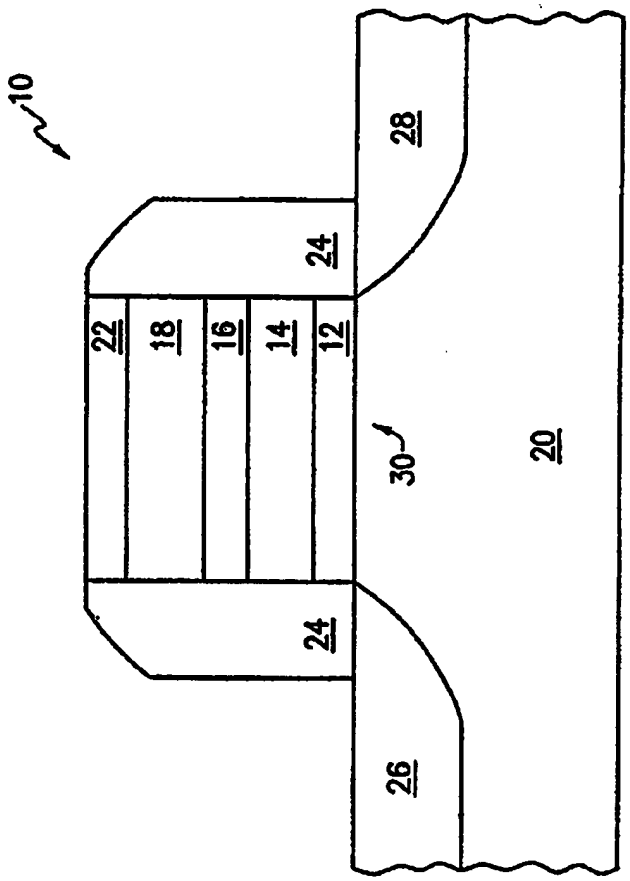


FIG. 1 (PRIOR ART)

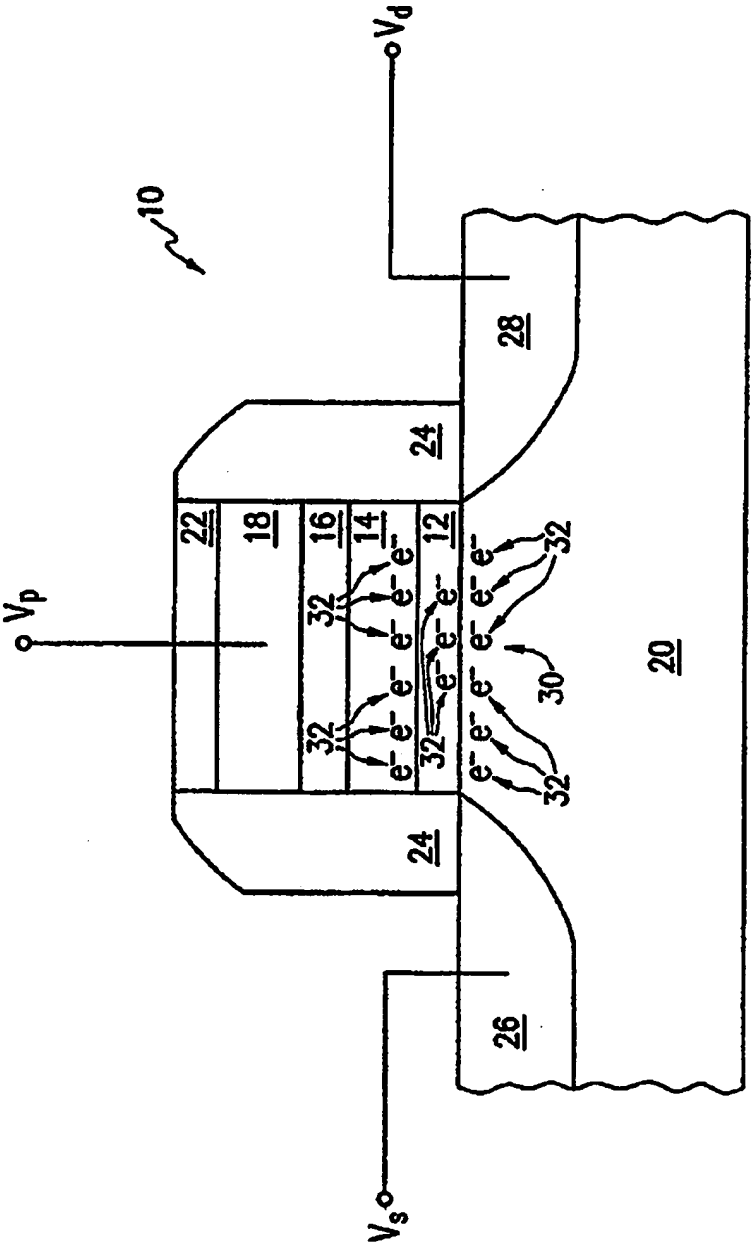


FIG. 2 (PRIOR ART)

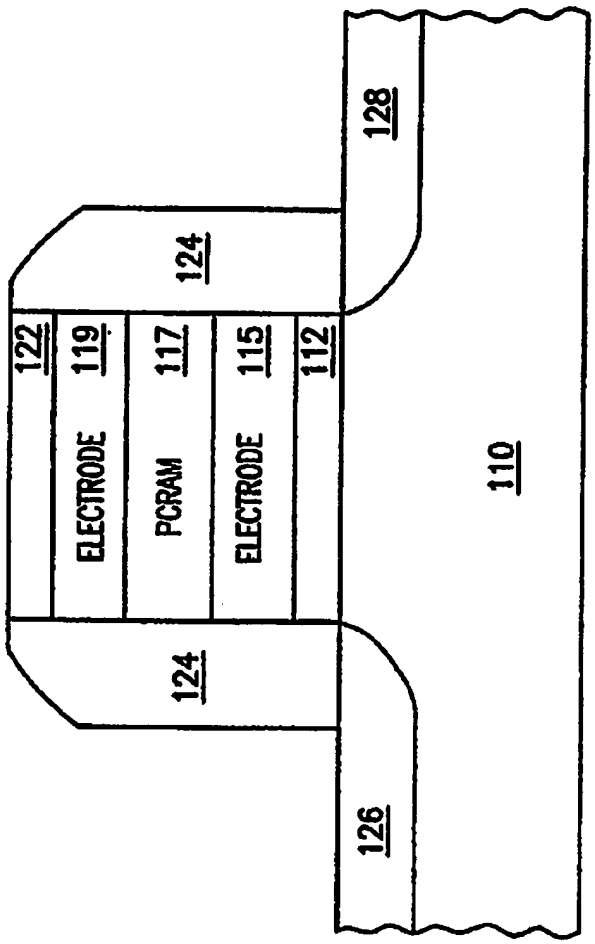

128
124
122
119
ELECTRODE
117
PCRAM
115
ELECTRODE
112
110
124
126

FIG. 3

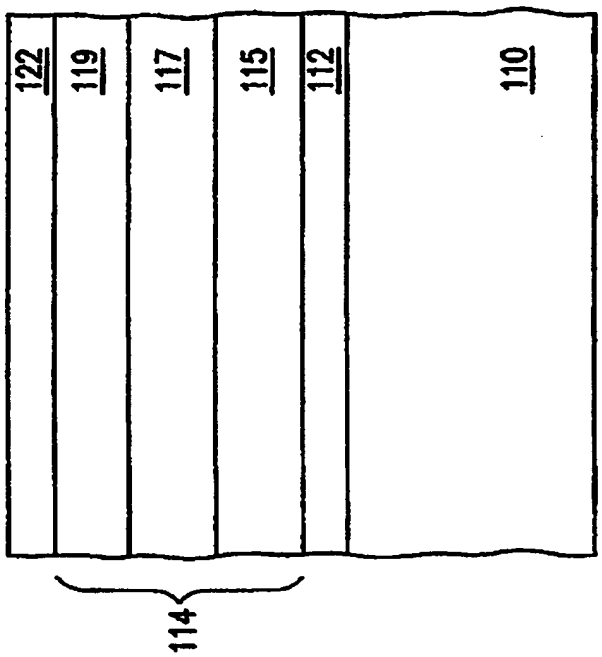


FIG. 4

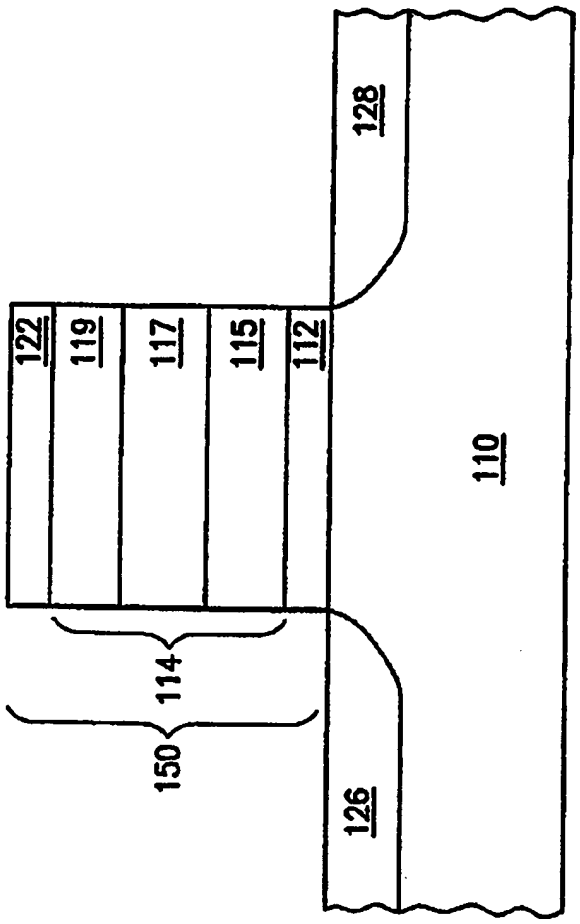


FIG. 5

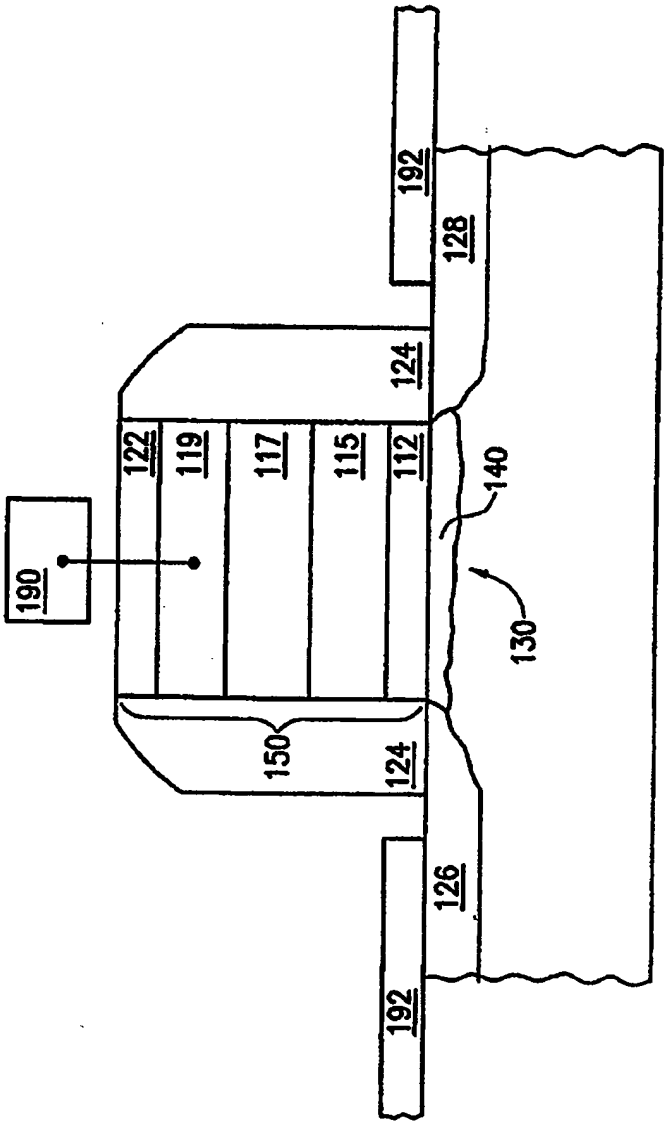


FIG. 6

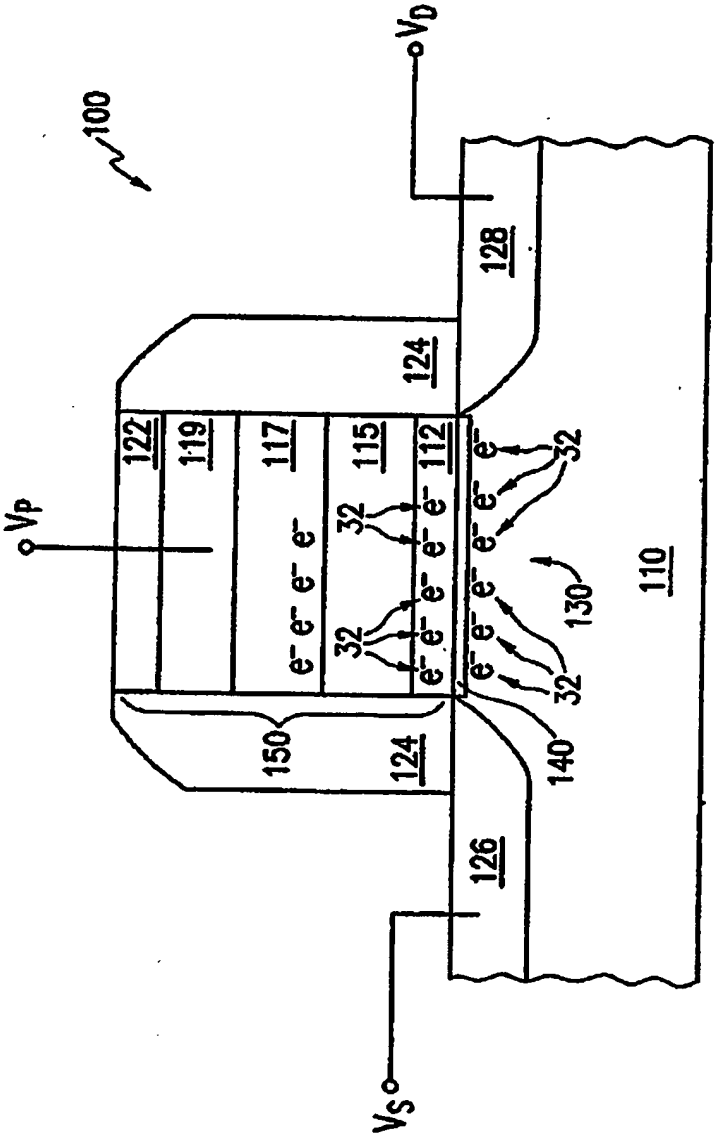


FIG. 7

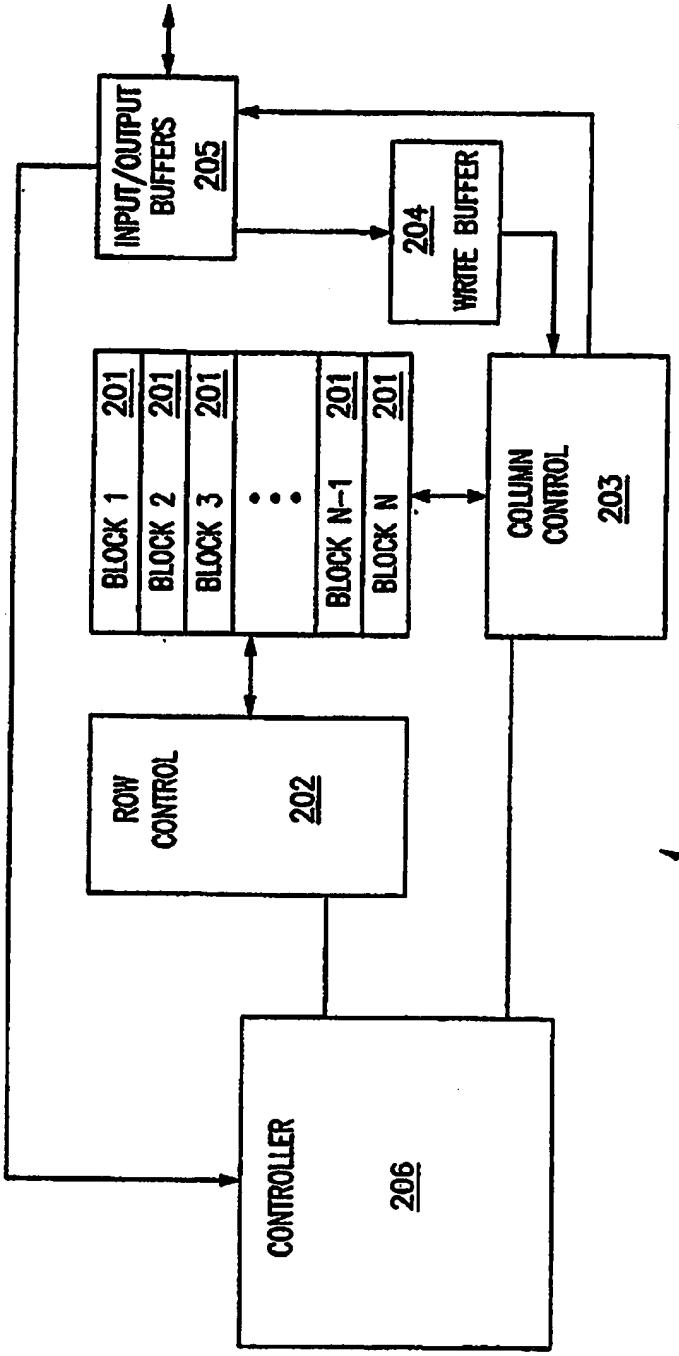

INPUT/OUTPUT BUFFERS 205
204 WRITE BUFFER
BLOCK 1 201
BLOCK 2 201
BLOCK 3 201
BLOCK N-1 201
BLOCK N 201
COLUMN CONTROL 203
ROW CONTROL 202
CONTROLLER 206
200

FIG. 8

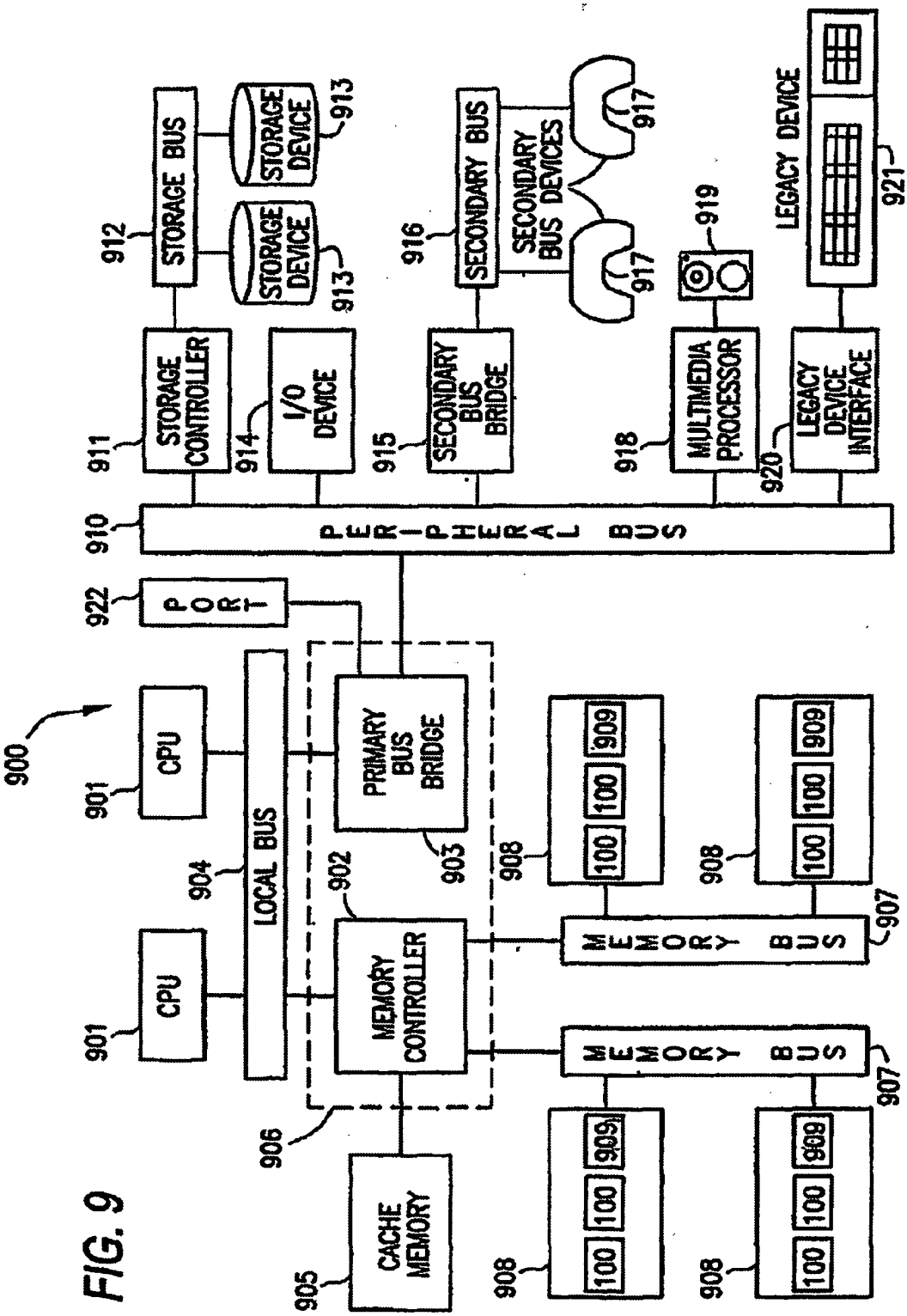

900
CPU
901
CPU
901
LOCAL BUS
904
PRIMARY BUS BRIDGE
903
MEMORY CONTROLLER
902
CACHE MEMORY
905
906
PORT
922
PERIPHERAL BUS
910
STORAGE CONTROLLER
911
I/O DEVICE
914
SECONDARY BUS BRIDGE
915
MULTIMEDIA PROCESSOR
918
LEGACY DEVICE INTERFACE
920
STORAGE BUS
912
STORAGE DEVICE
913
STORAGE DEVICE
913
SECONDARY BUS
916
SECONDARY BUS DEVICES
917
917
919
LEGACY DEVICE
921
MEMORY BUS
907
MEMORY BUS
907
908
908
908
908
909
100

FIG. 9